REMARKS

The above claims have been amended based upon the telephone conversation between Applicants' attorney and Examiner Harold Kim. The Examiner indicated that the memory clock divider circuit described and shown in Applicants' Specification is a memory clock tree circuit that generates branches of memory clock output signals. As such, the Examiner prefers the terms "tree" and "branches" instead of the term "divider". Applicants note that this terminology is consistent with Applicants' Specification (see, e.g., Specification, page 9, ll. 7-9 and elsewhere). As such, these amendments do not narrow the scope of the claims and the wording is inherent in the claims as filed. If the Patent Office is of a different view, Applicants respectfully request such a notification in writing.

Applicants respectfully submit that the Jones reference teaches, among other things, selecting one of several different clock frequencies depending upon the total bandwidth required by various functions of a graphics processor. Accordingly, among other differences, a single variable memory clock signal is used although its frequency may be varied. The memory clock signal of Jones is not branched into a plurality of independent clock signals that are coupled to a number of memory interface circuits for different processing engines as claimed. Also, among other differences, Fig. 4 of Jones is merely "clock control logic" which generates control signals. This circuit is not a clock tree circuit nor does it generate clock branches. To the contrary, the circuit of Fig. 4 generates control signals which act as select signals to select one of three different clock frequencies. For example, the outputs of comparatives 410, 411 and 412 are not independent clock signals divided from a memory clock but to the contrary, are control signals one of which selects an appropriate clock frequency, namely a clock frequency associated with CLK select 430, CLK/2 select 431 or CLK/4 select 432. As such, the control signal selects one of three different clock frequencies as the memory clock frequency, according, for example, to the table shown in Col. 4.

Moreover, the Jones reference teaches varying the memory frequency to the frame buffer. Jones does not mention a number of corresponding independent clock signals that have been branched from a memory clock, to a number of interface circuits for different processing engines of a graphics controller. Accordingly, the claims are also believed to be in condition for allowance for this reason.

In addition, Applicants claim, among other things, selectively activating at least some of the plurality of independent clock signals in response to received condition data during an active mode. As such, Applicants' invention turns on and off clock signals, namely a plurality of independent clock signals from the memory clock that go to differing graphics processor processing engines in response to received condition data, during an active mode.

Applicants also claim, among other things, selectively activating at least some of the plurality of independent clock signals. The cited portion of the Houston reference teaches an opposite approach, namely making it a non-zero frequency. In any event, Houston also fails to teach or suggest, among other things, a memory clock source for a graphics controller, and a memory clock tree circuit, that generates branches of memory clock output signals as a plurality of corresponding independent clock signals to a number of memory interface circuits for differing processing engines of a graphics controller and that selectively activates at least some of the plurality of independent clock signals in response to received condition data during an active mode. Accordingly, the claims are believed to be in condition for allowance.

Applicants also respectfully challenge the motivation to combine the teachings of Houston with those of Jones, since, among other things, Jones appears to use an opposite approach from that of Houston. Houston is directed to a system and method for reducing power dissipation in a circuit wherein an element of a circuit is identified and selected and an input to the element is altered to reduce the power dissipated by the element wherein, in particular, a logic component may determine an interval based on expired clock cycles or instructions processed. As such, the logic component evaluates instructions or the executable sequences of operations associated with specific elements. Such elements can then be selected for reduced power dissipation for a duration of the sequence of operations. The logic component may also utilize pattern recognition and pattern matching of a series of instructions as they are handled (see, e.g., Col. 7, ll. 14-62).

The Office Action attempts to combine the teachings of Jones with those of Houston. However, it is unclear which teachings from which reference are being combined. The Office Action states "it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the plurality of corresponding independent clock signals to a

number of interface circuits for differing processing engines and selectively activate at least some of the plurality of independent clock signals in response to received condition data during an active mode as shown in Houston for reducing power without impacting the operation the rest of the circuit." It is not clear which teaching from Jones is allegedly combinable with Houston. Applicants respectfully request a showing.

Moreover, Jones teaches away from Houston (and Applicants') claimed invention by, among other things, utilizing a single memory clock signal. It does not teach, suggest or contemplate splitting the memory clock signal into independent clock signals or in coupling those clock signals to the differing processing engines and selectively activating the independent clock signals. In fact, Jones teaches an opposite approach, namely a single variable frequency memory clock signal. It does not activate and deactivate multiple independent clock signals.

Also, Houston is not directed to a memory clock source, graphics controller, or memory clock divider circuit and teaches away from the structure of Jones. Accordingly, these references are not properly combinable. Applicants respectfully note that there does not appear to be any stated motivation in the record to combine the opposite teachings of these references. Accordingly, Claim 1 is believed to be in condition for allowance.

As to Claim 2, item 5 of Fig. 1 of Jones does not teach two different clock sources as claimed, namely a memory clock source and an engine clock source. Applicants respectfully submit that item 5 of Fig. 1 is the memory clock source that is not divided into independent clocks. There does not appear to be any teaching or suggestion of another engine clock source operatively coupled to a switching circuit to generate an output clock signal that is selectively coupled as a clock signal to a video overlay engine or video capture engine or any other graphics controller circuitry. Applicants respectfully request such a showing. In fact, it appears that Jones is silent as to a plurality of clocks as claimed. Accordingly, this claim is believed to be in condition for allowance.

As to Claim 3, Jones has previously been cited as teaching a variable memory clock control circuit operative to vary the speed of the memory clock based on the type of memory request from a plurality of memory requesters wherein the varying speed of the memory clock is passed through the memory clock divider circuit to generate a plurality of corresponding variable

independent clock signals. However, Applicants respectfully reassert the relevant remarks made above with respect to Claim 1 and again note that Jones fails to teach or suggest independent clocks split from the memory clock to processing engines and a variable memory clock control circuit that is operative to vary a speed of the memory clock and wherein the memory clock divider circuit divides the variable speed memory clock signals as a plurality of corresponding independent clock signals and selectively activates at least some of the plurality of independent clock signals in response to received condition data during an active mode. Accordingly, this claim is believed to be in condition for allowance.

As to Claim 7, Fig. 4 of Jones does not teach that a memory clock divider circuit includes a plurality of logic circuits wherein each logic circuit outputs one of the plurality of corresponding independent clock signals and each logic circuit is coupled to operatively receive different condition data.

With respect to Claim 4, Applicants respectfully submit that the data stored by the claimed read latch has already been read from a memory device (e.g., such as Houston). The Houston '101 reference describes a memory device, such as a DRAM, that includes an internal memory array and multiplexer block and control block, wherein the memory device includes internal latch blocks operable to receive a plurality of input signals that are operable to retain a plurality of data states and operable to provide an output signal. Hence, this reference is directed to circuits internal to the memory. In contrast, Applicants' memory latch circuits and memory latch control circuits as claimed in Claim 4 are external to and not part of the memory device that receives the memory clock signal but instead are coupled to receive data from the memory device. Applicants also respectfully request factual support for any alleged motivation to combine the Houston references with one another and the Houston '101 reference with that of Jones. Applicants respectfully submit that there is no suggestion or motivation to combine the teachings of the Houston references.

As to Claims 8-16, Applicants respectfully reassert the relevant remarks made above with respect to these claims.

Attached hereto is a marked up version of the changes made to the claims by the current amendment,. The attached page is captioned "Version With Markings to Show Changes Made."

Applicants respectfully submit that the claims are in condition for allowance and respectfully request that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

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By: Christopher J. Reckamp
Christopher J. Reckamp
Registration No. 34,414

VEDDER, PRICE, KAUFMAN &
KAMMHOLZ
222 N. LaSalle Street
Chicago, IL 60601
(312) 609-7599
FACSIMILE: (312) 609-5005

VERSION WITH MARKINGS TO SHOW CHANGES MADE

Please amend the claims to read as follows:

1. (Twice Amended) A power consumption reduction circuit comprising:

a memory clock source for a graphics controller; and

a memory clock [divider]tree circuit, operatively coupled to the memory clock source, that generates [divided]branches of memory clock output signals as a plurality of corresponding independent clock signals to a number of memory interface circuits for differing processing engines and selectively activates at least some of the plurality of independent clock signals in response to received condition data during an active mode.

7. (Once Amended) The circuit of claim 1 wherein the memory clock [divider]tree circuit includes a plurality of logic circuits, wherein each logic circuit outputs one of the plurality of corresponding independent clock signals and wherein each logic circuit is coupled to operatively receive different condition data associated with different condition data sources.

8. (Twice Amended) A power consumption reduction circuit comprising:

a memory clock source for a graphics controller;[and]

a memory clock [divider]tree circuit, operatively coupled to the memory clock source, that generates [divided]branches of memory clock output signals as a plurality of corresponding independent clock signals to a number of memory interface circuits for differing processing engines and selectively activates at least some of the plurality of independent clock signals in response to received condition data;

an engine clock source operatively coupled to a switching circuit that generates an output engine clock signal that is selectively coupled as a clock signal to each of a plurality of registers associated with at least one of: a video overlay engine, a video capture engine, I2C control logic and a multimedia port, such that the switching circuit disables the output engine clock signal in response to receiving condition data; and

a plurality of memory read latch circuits and a memory read latch control circuit operative to dynamically activate and de-activate the plurality of memory read latches based on detected memory read requests to facilitate memory access activity based power reduction.

12. (Once Amended) The circuit of claim 8 wherein the memory clock [divider]<u>tree</u> circuit includes a plurality of logic circuits, wherein each logic circuit outputs one of the plurality of corresponding independent clock signals and wherein each logic circuit is coupled to operatively receive different condition data associated with different condition data sources.

13. (Twice Amended) A power consumption reduction method comprising:

generating [divided]<u>branches of</u> memory clock output signals as a plurality of corresponding independent clock signals to a number of memory interface circuits for differing processing engines;

selectively activating at least some of the plurality of independent clock signals in response to received condition data;

selectively coupling an engine clock signal to each of a plurality of registers associated with at least one of: a video overlay engine, a video capture engine, I2C control logic and a multimedia port to selectively disable the output engine clock signal in response to receiving condition data; and

dynamically activating and de-activating a plurality of memory read latches based on detected memory read requests to facilitate memory access activity based power reduction.

16. (Once Amended) The method of claim 13 including:

outputting one of the plurality of corresponding independent clock signals from a different [divider]<u>branch</u> circuit based on receiving different condition data associated with different condition data sources.

17. (New) The circuit of claim 1, wherein the received condition data includes at least one of: CRT controller enable data, GUI active condition data, GUI write condition data, sub-picture "on" data, video capture enable data, half frame buffer data, and scaler enable data.

18. (New) The circuit of claim 8, wherein the received condition data includes at least one of: CRT controller enable data, GUI active condition data, GUI write condition data, sub-picture "on" data, video capture enable data, half frame buffer data, and scaler enable data.

19. (New) The method of claim 13, wherein the received condition data includes at least one of: CRT controller enable data, GUI active condition data, GUI write condition data, sub-picture "on" data, video capture enable data, half frame buffer data, and scaler enable data.